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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,193	08/18/2003	Azeez Bhavnagarwala	YOR920030289US1 (8728-635	3651

46069 7590 06/26/2008

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EXAMINER	
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ART UNIT	PAPER NUMBER
2857	

MAIL DATE	DELIVERY MODE
06/26/2008	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/643,193
Filing Date: August 18, 2003
Appellant(s): BHAVNAGARWALA ET AL.

Nathaniel T. Wallace
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed March 28, 2008, appealing from the Office action mailed January 09, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is substantially correct. While Appellant indicates that claims 17 and 37 are allowable, claims 17 and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,275,094	CRANFORD, JR. ET AL	08-2001
6,731,916	HARUYAMA	05-2004
5,999,043	ZHANG ET AL	12-1999
6,819,183	ZHOU ET AL	11-2004
4,851,768	YOSHIZAWA ET AL	07-1989
6,181,621	LOVETT	01-2001
6,798,278	UEDA	09-2004

Conti et al., "Test structure for mismatch characterization of MOS transistors in subthreshold regime"

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3, 5-10, 12, 26, 27, 29, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,275,094 to Cranford, Jr. et al. in view of

Conti et al., "Test structure for mismatch characterization of MOS transistors in subthreshold regime".

With respect to claim 1, Cranford, Jr. discloses a method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices (column 7, lines 4-9) wherein the DC voltage characteristic data comprises an output DC voltage (column 7, lines 7-9 and column 8, lines 1-4) as a function of an input DC voltage (column 7, lines 14-16) wherein the input voltage is applied to a gate of at least one of the first and second semiconductor transistors (column 7, lines 14-16) and wherein the output voltage is obtained at a common node connection of the first and second semiconductor transistor devices (column 7, lines 7-9) and processing the DC voltage characteristic data to determine a distribution of device mismatch between the semiconductor devices (column 7, lines 20-23 and 28-36).

With respect to claims 3 and 29, Cranford, Jr. discloses that the distribution of device mismatch comprises a distribution threshold voltage mismatch (column 7, lines 28-36).

With respect to claims 6, 12, and 32, Cranford, Jr. discloses that the step of obtaining DC voltage characteristic data for the device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs (i.e. either p-type pairs or n-type pairs) (column 7, lines 4-9).

With respect to claim 7, Cranford, Jr. discloses determining a variation in a device characteristic for a device of the integrated circuit comprising the device pair (column 1, lines 6-20 and column 4, lines 9-20).

With respect to claim 8, Cranford, Jr. discloses accessing random variation of device mismatch of the semiconductor integrated circuit (column 1, lines 6-20 and column 4, lines 9-20) using variations in the device characteristic for each device of the integrated circuit (i.e. each pair) (column 7, lines 4-9) as determined from distributions of variation of device mismatch for device pairs within the integrated circuit (column 7, lines 20-23 and 28-36).

With respect to claim 9, Cranford, Jr. discloses that the device characteristic comprises threshold voltage (column 7, lines 28-36).

With respect to claim 10, Cranford, Jr. discloses a method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of obtaining DC voltage characteristic data (column 7, lines 7-9 and column 8, lines 1-4) for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors (column 7, lines 4-9) in the integrated circuits (column 1, lines 6-20 and column 4, lines 9-20) wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage (column 7, lines 7-9 and column 8, lines 1-4) as a function of an input DC voltage (column 7, lines 14-16) wherein the input voltage is applied to a gate of at least one of the first and second transistors (column 7, lines 14-16) and wherein the output voltage is obtained at a common node connection of the first and second

transistors (column 7, lines 7-9) and determining a distribution of threshold voltage mismatch for the a selected device pair using corresponding DC voltage characteristic data for the selected device pair (column 7, lines 20-23 and 28-36), determining a threshold variation of transistors in the integrated circuit using one or more determined distributions of threshold voltage mismatch for selected device pairs (column 1, lines 6-10 and column 7, lines 20-23 and 28-36), and characterizing random variations of the integrated circuit using one or more determined threshold variations of transistors of the integrated circuit (column 1, lines 6-20, column 4, lines 9-20 and column 7, lines 20-23 and 28-36).

With respect to claims 26 and 27, Cranford, Jr. discloses implementing the method using a program storage device readable by a machine tangibly embodying a program of instructions (column 7, lines 26-28).

Cranford, Jr. further discloses that the threshold voltage mismatch between the first and second transistors is when the first and second transistors each comprise an NFET (column 7, lines 4-9).

As noted above, the invention of Cranford, Jr. teaches many of the features of the claimed invention and while Cranford, Jr. does teach obtaining DC voltage characteristic of a transistor pair, Cranford, Jr. does not explicitly state that the transistors are operating in a subthreshold region.

Conti teaches a test structure for threshold voltage mismatch comprising obtaining subthreshold DC voltage characteristic data for adjacent transistor devices (page 173, column 1, “Introduction, lines 1-9 and page 173, column 2, “Mismatch

Model", lines 9-13) by biasing the transistors in a subthreshold region through application of corresponding gate voltages (page 173, "Test Circuits" and page 174, column 1, lines 1-7).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. to include obtaining the DC voltage characteristic for a transistor pair operating in a subthreshold region, as taught by Conti, because, as suggested by Conti, the combination would have improved the analysis and control of mismatch by providing a better estimate of threshold mismatch (page 173, column 1, Introduction, lines 7-9 and page 174, column 1, lines 1-7).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti and in view of U.S. Patent No. 6,731,916 to Haruyama.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does obtain DC voltage characteristic data for a pair of transistors, the combination does not specify retrieving this data from a database.

Haruyama teaches a power amplifying apparatus for a mobile phone including an FET with a bias current setting circuit (column 3, lines 9-11) and a memory/database (column 3, lines 11-13) wherein voltage characteristic data for the FET is stored in the memory/database (column 3, lines 14-20) and, when needed, is retrieved from the memory/database (column 3, lines 42-47).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to include retrieving the DC voltage characteristic data from a database, as taught by Haruyama, because the invention of Cranford, Jr. and Conti does teach storing the DC voltage data in a look-up table and Haruyama suggests that the combination would have saved time and effort by storing the characteristic data in a database (column 3, lines 14-20 and column 3, lines 42-47) thereby not requiring the process of measuring the characteristic data each time the mismatch is to be determined in the invention of Cranford, Jr. and Conti.

Claims 13 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and further in view of U.S. Patent No. 5,999,043 to Zhang et al.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does teach maintaining the transistor pair in a subthreshold region, the combination does not explicitly describe varying the gate voltages of the transistors to obtain such subthreshold operation.

Zhang teaches an on-chip high resistance device for passive low pass filters with programmable poles comprising a transistor device that is controlled to operate in a subthreshold region through variation in the voltage applied to the gate (column 3, lines 46-49).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to explicitly describe varying the gate voltages of the transistors to obtain such subthreshold operation, as taught by Zhang, because the combination of Cranford, Jr. and Conti does teach maintaining the transistor pair in a subthreshold region and Zhang suggests a corresponding method for controlling the transistors to maintain such subthreshold operation, as needed in the invention of Cranford, Jr. and Conti, to obtain accurate threshold voltage mismatch measurements (column 3, lines 46-49).

Claims 11 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and Zhang et al. and further in view of U.S. Patent No. 6,819,183 to Zhou et al.

As noted above, Cranford, Jr. in combination with Conti and Zhang teaches many of the features of the claimed invention and while the invention of Cranford, Jr., Conti, and Zhang does teach maintaining the transistor pair in a subthreshold region by varying gate voltages as needed, the combination does not explicitly describe keeping the gate voltages of the transistors constant to obtain such subthreshold operation.

Zhou teaches temperature and process compensation of MOSFETs operating in sub-threshold mode wherein a level of a current source is set to maintain a gate voltage of the MOSFET at a constant below its threshold voltage, thereby maintaining operation in a subthreshold region (column 6, lines 17-21).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr., Conti, and Zhang to explicitly describe keeping the gate voltages of the transistors constant to obtain such subthreshold operation, as taught by Zhang, because the combination of Cranford, Jr., Conti, and Zhang does teach maintaining the transistor pair in a subthreshold region by varying gate voltages as needed and Zhang suggests another method for controlling the transistors to maintain such subthreshold operation, as needed in the invention of Cranford, Jr., Conti, and Zhang, when the devices are already operating in a subthreshold region and do not require any variation to obtain accurate threshold voltage mismatch measurements (column 6, lines 17-21).

Claims 15, 16, 35, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and further in view of U.S. Patent No. 4,851,768 to Yoshizawa et al.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention, and while the invention of Cranford, Jr. and Conti does teach determining a distribution of threshold voltage mismatch as a function of input and output voltages in a look-up table (Cranford, Jr.; column 7, lines 20-23 and 28-36), the combination does not explicitly indicate whether a distribution of input voltages is given for a particular output voltage.

Yoshizawa teaches a characteristic test apparatus for an electronic device comprising a transistor pair configured with a node for measuring an output voltage,

that varies as a function of the input voltage, between the first and second transistors (Figure 2a) wherein a varying/distribution of input voltages are applied to obtain voltage output to determine a threshold voltage as part of a DC voltage characteristic (column 4, lines 59-67) wherein the threshold voltage can be determined either by determining the distribution of input voltages for a given output voltage or determining a distribution of output voltages for a given input (column 6, lines 6-17).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to explicitly include a distribution of input voltages for a particular output voltage, as taught by Yoshizawa, because the invention of Cranford, Jr. and Conti does provide a distribution of threshold voltage mismatch as a function of input and output voltages in a look-up table and Yoshizawa suggests a corresponding method for determining such a distribution that would have aided the user by implementing known relationships between input/output voltage and threshold mismatch to allow the user to determine threshold voltage mismatches as part of the look-up table using either known input voltage levels or known output voltage levels as available (column 4, lines 59-67 and column 6, lines 6-17).

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. in view of Conti and further in view of U.S. Patent No. 6,181,621 to Lovett.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does teach characterizing mismatch in a semiconductor integrated circuit, the combination does not specify that the integrated circuit be an SRAM.

Lovett teaches a threshold voltage mismatch compensated sense amplifier for SRAM memory arrays comprising means for obtaining threshold voltage mismatch information in a SRAM (column 1, lines 6-10 and column 2, lines 7-15).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to specify that the integrated circuit be an SRAM, as taught by Lovett, because the invention of Cranford, Jr. and Conti does teach employing a threshold voltage mismatch compensated sense amplifier (Cranford, Jr.; column 7, lines 4-5 and 20-23) and Lovett suggests that SRAM devices are devices that employ compensated sense amplifiers (column 1, lines 6-10) and are greatly affected by threshold mismatches due the size constraints of such SRAMs (column 3, line 65 to column 4, line 7) and therefore the combination would have provided greater utility in the invention of Cranford, Jr. and Conti by applying the method to the SRAM devices.

Further, it has been held that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136

USPQ 458, 459 (CCPA 1963). In the instant case the structure of Cranford, Jr. and Conti is capable of characterizing transistor mismatch in any of a wide variety of integrated circuits, such as an SRAM, and therefore meets the claim.

Claims 19 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and further in view of U.S. Patent No. 6,798,278 to Ueda.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does teach a determining a voltage threshold variation of transistors in an integrated circuit using a microprocessor measuring an output voltage as a function of an input voltage, the combination does not specifically indicate determining the variation by determining a standard deviation of threshold voltage variation of the transistors.

Ueda teaches a voltage reference generation circuit and power source incorporating such a circuit wherein a variation in threshold voltage mismatch is determined for a transistor pair by determining a standard deviation (column 13, lines 28-41).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to specifically determine a standard deviation of threshold voltage variation of the transistors, as taught by Ueda, because the invention of Cranford, Jr. and Conti does teach determining threshold voltage mismatch indicating the similarity of the transistors using a processor that corrects

for the voltage mismatch and Ueda suggests a corresponding conventional method for determining such variation that would have expressed the variation in terms of a standard deviation that is comparable to accepted limits, thereby increasing the efficiency of the invention of Cranford, Jr. and Conti, by allowing the processor to determine when the variation is outside such limits and the correction needs to be performed (column 13, lines 28-41).

(10) Response to Argument

The Examiner first asserts that, as indicated in the Pre-Brief Appeal Conference decision mailed June 25, 2007, the rejection of claims 1, 3-13, 15-19, 26, 27, 29, and 32-38 under 35 U.S.C. 101 has been withdrawn.

With respect to the outstanding 35 U.S.C. 103(a) rejections, Appellant first argues:

> With regard to Claims 1, 10, 26 and 27, Applicants contend that the combination of Cranford and Conti does not teach or fairly suggest a process for characterizing device mismatch in a semiconductor integrated circuit, comprising, for example, *obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region, and processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices*, as essentially claimed in Claims 1, 10, 26 and 27.
>
> In formulating the obviousness rejection of claim 1, for example, the Examiner relies primarily on the teachings of Cranford as anticipating the above elements of claim 1 (see page 5 of the Final Action) and relying on Conti as teaching a test structure for threshold voltage mismatch using subthreshold DC voltage characteristic data (see page 8 of the Final Action). However, the Examiner's reliance of the teachings of Cranford and Conti in this regard is wholly misplaced
>
> For example, on page 5 of the Final Office Action, the Examiner essentially contends that Cranford teaches *obtaining DC characteristic data for a device pair*

(Col. 7, lines 4-9, Col. 8, lines 1-4) *comprising an output DC voltage as a function of an input DC voltage* (col. 7, lines 14-16) and processing the DC voltage characteristic data to determine a distribution of device mismatch (Col. 7, lines 20-23 and 28-36). The Examiner's reliance on the cited sections of Cranford in this regard is technically erroneous as a matter of fact.

Cranford teaches in the cited sections a method for dynamically generating a voltage to correct threshold mismatch between transistor devices in a differential amplifier to thereby correct for manufacturing offset (See Abstract; and Col. 7, lines 20-23). Cranford explains that this is done by performing a Fast Fourier Transform analysis to identify harmonic differences in the AC input-output signals at input and output terminals to determine mismatch between input and output harmonics where any mismatch is translated into a voltage representative of the offset between the differential transistor pair, and where the feedback voltage is returned to the differential pair to eliminate the effect of offset (see, Col. 4, lines 34-44).

Cranford teaches (in Col 7, lines 44-55 that the input signals (160) and (162) input to terminals 112 and 114 and output signals of terminals 116 and 120 are AC sinusoidal signals that are analyzed for purposes of determining threshold voltage offset (see, AC signals of FIG. 6). Moreover, Col. 8, lines 1-4 of Cranford states that:

> **FIG. 8 shows the change in various harmonics in the output signal 163 after the offset voltage supplied by the feedback circuit 150 is provided to the transistors connected to the output terminal 116, 120 (see FIG. 5).**

FIG. 8 is nothing more than a representation of the offset in FIG. 7 in terms of amplitude and frequency for the various harmonics in the output signal prior to correction of offset voltage (see, Col, 5, lines 4-6). In other words, FIG. 8 illustrates Amplitude (in db) of the output signal as a function of Frequency (*i.e., Output Voltage Amplitude vs. Frequency*).

In view of the above, the Examiner's assertion that Cranford teaches ***obtaining DC voltage characteristic data*** *for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage Vout as a function of an input DC voltage Vin, wherein Vin is applied to a gate of at least one of the first and second semiconductor transistor devices and wherein Vout is obtained at a common node connection of the first and second semiconductor transistor devices* lacks support.

At most Cranford teaches a process of determining/correcting threshold voltage offset using FFT analysis of the harmonics of AC input-output sinusoidal signals, which are clearly distinct from the claimed invention of obtaining and using DC voltage characteristic data to determine device mismatch.

The Examiner's interpretation of FIG. 8 of Cranford as disclosing **DC voltage Vout as a function of an input DC voltage Vin**, is misplaced, especially given the clear and explicit teachings of Cranford as to what FIG. 8 represents. Further,

> the Examiner fails to explain how a *process of correcting threshold mismatch by performing a fast Fourier transform analysis to detect harmonic differences identified by the FFT between sinusoidal input-output signals* as taught by Cranford is even remote the same or similar to the claimed process of *processing the DC voltage characteristic data* (which is *output DC voltage Vout as a function of an input DC voltage Vin) to determine a distribution of device mismatch between the first and second semiconductor transistor devices* as claimed in Claims 1 and 26, for example.
>
> Indeed, it is clear that Cranford does not teach the use of DC *voltage characteristic* data as claimed to determine device mismatch, but rather the use of FFT analysis of AC input-output signals to determine differences in harmonics of sinusoidal input-output voltages and correlate the differences to device offset. In this regard, the Examiner's arguments as premised on Cranford are fundamentally flawed on technical and legal grounds.

First, the Examiner asserts that Appellant explicitly admits that "Cranford teaches in the cited sections a method for dynamically generating a voltage to correct threshold mismatch between transistor devices in a differential amplifier to thereby correct for manufacturing offset". Therefore, by admitting that Cranford teaches generating a voltage to correct for threshold mismatch that is attributed to offset, Appellant is admitting that Cranford teaches voltage characteristic data to correct for threshold mismatch offset. The Examiner asserts that Cranford also explicitly states that this voltage to correct for threshold mismatch offset is DC voltage:

> FIG. 8 shows the change in the various harmonics in the output signal 163 after the offset voltage supplied by the feedback circuit 150 is provided to the transistors connected to the output terminals 116, 120 (See FIG. 5). Specifically, the DC component in the output has been essentially removed while the first and third harmonics are essentially at the same amplitude as in FIG. 7 (column 8, lines 1-7)

Second, Appellant argues that "Cranford explains that this is done by performing a Fast Fourier Transform analysis to identify harmonic differences in the AC input-

output signals at input and output terminals to determine mismatch between input and output harmonics where any mismatch is translated into a voltage representative of the offset between the differential transistor pair, and where the feedback voltage is returned to the differential pair to eliminate the effect of offset (see, Col. 4, lines 34-44)" and "Cranford teaches (in Col 7, lines 44-55 that the input signals (160) and (162) input to terminals 112 and 114 and output signals of terminals 116 and 120 are AC sinusoidal signals that are analyzed for purposes of determining threshold voltage offset (see, AC signals of FIG. 6)", apparently to attempt to point out that by disclosing AC signals, Cranford does not teach DC voltage characteristic data.

In response, the Examiner asserts that Appellant's arguments are with respect to the term "DC voltage characteristic data". Such a term is interpreted to mean any data that pertains to DC voltage and, as such, does not imply isolated DC data. Additionally, the Examiner asserts that one having ordinary skill in the art would recognize that, in most applications, an AC signal contains a non-zero DC component, and therefore Appellant's arguments that the signals obtained in Cranford are AC, is not considered to be persuasive. Further, the Examiner asserts that Cranford explicitly indicates that the signals described by Appellant as "AC sinusoidal signals that are analyzed for purposes of determining threshold voltage offset (see, AC signals of FIG. 6)" contain such a DC component, specifically:

> FIG. 7 shows in more detail the various harmonics occurring in the output signal 163 before offset correction. At 0 frequency the output signal includes a DC component of approximately -32 dB. The fundamental harmonic has amplitude of -24 dB and occurs at 10 mHertz. The second harmonic has

> amplitude of -58 dB and occurs at 20 mHertz. The third harmonic has amplitude of -65 dB and occurs at 30 mHertz. The fourth through 10th harmonics are shown in the remainder of the graph. The even harmonics indicates distortion has been introduced by the threshold mismatch between n type devices 29, 28 (column 7, lines 57-67)

Additionally, in response to Appellant's argument against Cranford teaching obtaining DC characteristic data by indicating that "FIG. 8 shows the change in various harmonics in the output signal 163 after the offset voltage supplied by the feedback circuit 150 is provided to the transistors connected to the output terminal 116, 120 (see FIG. 5)", "FIG. 8 is nothing more than a representation of the offset in FIG. 7 in terms of amplitude and frequency for the various harmonics in the output signal prior to correction of offset voltage", and "The Examiner's interpretation of FIG. 8 of Cranford as disclosing **DC voltage Vout as a function of an input DC voltage Vin**, is misplaced, especially given the clear and explicit teachings of Cranford as to what FIG. 8 represents", the Examiner again asserts that Cranford is explicit in disclosing that signal 163 includes a DC component (i.e. DC voltage characteristic data) as noted above. The Examiner also asserts that Appellant is neglecting to summarize the entire discussion of Figure 8 as provided by Cranford, specifically that Cranford discloses that Figure 8 illustrates the resulting threshold voltage offset compensation that removes the DC component in the measured output, specifically:

> FIG. 8 shows the change in the various harmonics in the output signal 163 after the offset voltage supplied by the feedback circuit 150 is provided to the transistors connected to the output terminals 116, 120 (See FIG. 5). Specifically, the DC component in the output has been essentially removed while the first and third harmonics are essentially at the same amplitude as in FIG. 7. The even

> harmonics have essentially dropped out of the output signal. Without the presence of the even harmonics due to the offset voltage provided by the feedback circuit 150, the output signal 163 is the same as the input signals 160, 162 as shown in FIG. 6 (column 8, lines 1-12)

In light of the above, the Examiner asserts that Appellant's argument that by disclosing AC signals, Cranford cannot teach the claimed aspects of DC voltage characteristic data is misguided. Instead, the Examiner maintains that Cranford discloses a method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices (column 7, lines 4-9) wherein the DC voltage characteristic data comprises an output DC voltage (column 7, lines 7-9 and column 8, lines 1-4) as a function of an input DC voltage (column 7, lines 14-16) wherein the input voltage is applied to a gate of at least one of the first and second semiconductor transistors (column 7, lines 14-16) and wherein the output voltage is obtained at a common node connection of the first and second semiconductor transistor devices (column 7, lines 7-9) and processing the DC voltage characteristic data to determine a distribution of device mismatch between the semiconductor devices (column 7, lines 20-23 and 28-36).

These cited sections of Cranford state:

> Turning to FIG. 4, a differential amplifier 100 incorporating CMOS transistors 102 and 104 (shown in FIGS. 1A and C) have p type devices 7, 25 coupled to n type devices 29, 28 through their common drain electrodes. An output circuit 118 is coupled to the common drain electrodes 116, 120. (column 7, lines 4-9)

> The n type devices 29, 28 gate electrodes are connected to an input positive signal 114 and an input minus signal 112, respectively. (column 7, lines 14-16)

> FIG. 5 shows one example of a voltage feedback circuit 150 which automatically generates a voltage for correction of the threshold mismatch between n type device 28 and 29 as a result of manufacture. (column 7, lines 20-23)
>
> The Fast Fourier Transforms (FFT) application is executed for detection of harmonic differences between the signals at the input and output terminals and introduced by threshold offset which is a well-known technique. Based on the harmonic differences identified by the FFT in the input-output signals and indicative of the offset between the n type devices 29, 28, the table 156 can be constructed to indicate a voltage level to correct the offset. (column 7, lines 28-36)
>
> FIG. 8 shows the change in the various harmonics in the output signal 163 after the offset voltage supplied by the feedback circuit 150 is provided to the transistors connected to the output terminals 116, 120 (See FIG. 5). (column 8, lines 1-4)

Therefore, the Examiner maintains that Cranford discloses a device pair comprising first and second semiconductor transistor devices (i.e. nFETs N28 and N29), obtaining DC voltage characteristic data for the device pair (i.e. input and output signals obtained by the microprocessor as part of the voltage feedback circuit) wherein the DC voltage characteristic data comprises an output DC voltage VOUT a function of an input DC voltage VIN (i.e. the DC offset voltage measured in the voltage feedback circuit as a function of the input voltage applied to the transistors), wherein VIN is applied to a gate of at least one of the first and second semiconductor transistor devices (i.e. inputs 112/114 applied to nFET gate) and wherein VOUT is obtained at a common node connection of the first and second semiconductor transistor device (i.e. common outputs 116/120).

The Examiner maintains that the description of Figure 8 describes that the DC offset voltage of the voltage amplitude of the semiconductor transistor pair has been

correctly compensated. This compensation is the threshold voltage mismatch that has been determined from the obtained VIN and VOUT and therefore, since one having ordinary skill in the art would recognize that in order to determine DC voltage offset between two transistor devices, the DC voltage offset must first be measured, this description, in combination with the other cited sections of Cranford, does disclose DC voltage VOUT as a function of an input DC voltage VIN.

Finally, in response to Appellant's argument that "the Examiner fails to explain how a *process of correcting threshold mismatch by performing a fast Fourier transform analysis to detect harmonic differences identified by the FFT between sinusoidal input-output signals* as taught by Cranford is even remote the same or similar to the claimed process of *processing the DC voltage characteristic data* (which is *output DC voltage Vout as a function of an input DC voltage Vin) to determine a distribution of device mismatch between the first and second semiconductor transistor devices* as claimed in Claims 1 and 26", the Examiner maintains that, as explained above, the input-output signals of Cranford clearly contain DC voltage characteristic data. Additionally, Cranford specifically discloses creating a table of offset voltages to determine, and subsequently correct, a distribution of threshold voltage mismatch between the first and second semiconductor transistor devices, specifically:

> FIG. 5 shows one example of a voltage feedback circuit 150 which automatically generates a voltage for correction of the threshold mismatch between n type device 28 and 29 as a result of manufacture. The circuit 150 includes a microprocessor 151 coupled to the input terminals 114 and 112 and to

the output terminals 116 and 120 (See FIG. 4). The processor 151 includes a memory 152 which stores an operating system 153, a Fast Fourier Transform application 154, and an offset table 156. The Fast Fourier Transforms (FFT) application is executed for detection of harmonic differences between the signals at the input and output terminals and introduced by threshold offset which is a well-known technique. Based on the harmonic differences identified by the FFT in the input-output signals and indicative of the offset between the n type devices 29, 28, the table 156 can be constructed to indicate a voltage level to correct the offset. The processor scans the table and provides an output signal level to control a voltage supply 158 coupled to the n type devices 29, 28 back bias contacts 36. In response to the signal level, the voltage supply adjusts the potential of the back bias contacts to correct for the offset representative of the threshold mismatch between the n type devices 29, 28 introduced during manufacture of the devices. (column 7, lines 20-43).

Appellant argues:

In any event, on page 8 of the Final Office Action, the Examiner admits that Cranford does **not teach** obtaining DC voltage characteristic data of a transistor pair when the transistors are operating in the sub-threshold region. In this regard, the Examiner essentially acknowledges that Cranford does not teach every feature of the claimed inventions of Claims 1, 10, 26, and 27. Instead, the Examiner relies on Conti as teaching "obtaining subthreshold DC voltage characteristic data for adjacent transistors" contending that it would be obvious to modify the teachings of Cranford to include the use of DC voltage characteristic data of a transistor pair operating in the subthreshold regime as taught by Conti

The Examiner's reliance on Conti in this regard is *grossly* misplaced on two fundamental levels. First, *Conti* teaches a mismatch model based on measurements of drain current ID (see page 173, second column on bottom). The Examiner seemingly misunderstands the *fundamental difference* between **DC Voltage characteristic data** (as claimed) and **DC Current characteristic data** (as disclosed in Conti). In fact, as presented at pages 6-9 of the Background section of Applicants' specification, there are problems associated with the use of DC Current characteristic data (as taught by Conti) for purposes of evaluating device mismatch. In this regard, Conti clearly teaches away from the claimed invention and renders the rejection legally deficient on its face.

Moreover, the Examiner takes a leap to explain motivation for modifying Cranford with Conti. Again, Cranford does not teach DC voltage characteristic data to determine device mismatch, but rather FFT analysis of AC signals. Moreover, Cranford's process of correction of mismatch is not compatible with the transistor pairs under consideration being operated in the "subthreshold regime." Cranford teaches a real-time correction process in which the transistor

> pairs under consideration are not biased to operate in the subthreshold regime (or the circuit would not work). The proposed combination of Conti and Cranford as applied to Claims 1, 10, 26, and 27 in this regard is not tenable for at least the above reasons. Thus, withdrawal of the rejection of Claims 1, 10 26 and 27 is respectfully requested.

First, the Examiner asserts that the invention of Conti is not relied upon for any teaching regarding measurement of drain current. Rather, the Final Office Action set forth that while "the invention of Cranford, Jr. teaches many of the features of the claimed invention and while Cranford Jr. does teach obtaining DC voltage characteristic of a transistor pair, Cranford, Jr. does not explicitly state that the transistors are operating in a subthreshold region." Therefore, the invention of Conti is only relied upon to modify the invention of Cranford to include obtaining the DC voltage characteristic, as taught by Cranford, for a transistor pair operating in a subthreshold region. As such, since there is nothing in Cranford that explicitly or implicitly indicates that the transistors of Cranford, cannot and/or should not operate in a subthreshold region, the Examiner asserts that Conti does not constitute a teaching away.

Second, in response to Appellant's argument that "Cranford's process of correction of mismatch is not compatible with the transistor pairs under consideration being operated in the 'subthreshold regime'" because "Cranford teaches a real-time correction process in which the transistor pairs under consideration are not biased to operate in the subthreshold regime (or the circuit would not work)", the Examiner asserts that Appellant has not provided any reasoning or evidence to support such an assertion that the circuit of Cranford would not work if the transistors were biased

to operate in the subthreshold regime. As such, the Examiner does not consider such arguments to be persuasive.

Instead, the Examiner maintains that it would have been obvious to one having ordinary skill in the art to modify the invention of Cranford to include obtaining the DC voltage characteristic for a transistor pair operating in a subthreshold region, as taught by Conti, because, as suggested by Conti, the combination would have improved the analysis and control of mismatch by providing a better estimate of threshold mismatch (page 173, column 1, Introduction, lines 7-9 and page 174, column 1, lines 1-7). Specifically, the Examiner maintains that the invention of Conti specifically indicates that "mismatch characterization of MOS transistor operating in subthreshold regime becomes extremely important for an accurate design" (page 173, column 1, Introduction, lines 7-9) and "estimation of ΔV_{TH} is more accurate in subthreshold rather than in saturation regime, since the effect on I_D or a variation of V_{TH} is more pronounced as can be seen…" (page 174, column 1, lines 1-7).

Since Cranford teaches obtaining the DC output voltage characteristic data from a common node terminal connecting the transistor pair drain terminals (Cranford; column 7, lines 7-9) and since it is well known that the output voltage is directly proportional to the output current, Conti suggests that operating the transistors in the subthreshold region would have provided more pronounced mismatch determination in the voltage characteristic of Cranford. Therefore, the Examiner's reliance upon Conti is not for any measurements of drain current. Instead, the Examiner is relying on a teaching that that operating transistors in the subthreshold region provides

more pronounced mismatch determination. Since output voltage is directly proportional to output current, this more pronounced mismatch occurs when drain voltage is measured as well when drain voltage is measured and therefore is applicable to the invention of Cranford.

With respect to the rejections of claims 4, 11, 13, 15, 16, 18, 19, 33-36, and 38, in further view of Haruyama, Zhang et al., Zhou et al., Yoshizawa et al., Lovett, and/or Ueda, Appellant provides no new arguments, rather arguing that these claims should be allowable due to the argued combination of Cranford and Conti. Since the Examiner maintains the combination of Cranford and Conti, as explained above, Appellants arguments with respect to claims 4, 11, 13, 15, 16, 18, 19, 33-36, and 38 are not considered to be persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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